14.3 A 630MHz Direct Digital Frequency Synthesizer with 90dBc SFDR in 0.25μm CMOS

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The basic architecture of a Direct Digital Frequency Synthesizer (DDFS) is shown in Fig. 14.3.1. The most critical DDFS elements are the sine and cosine computation blocks that compute the two functions: $f(x)=\sin(\pi/4\cdot x)$, $g(x)=\cos(\pi/4\cdot x)$. The remaining blocks in the sine cosine generator use the symmetry of trigonometric functions to reconstruct the full-wave sine and cosine waveforms. The truncated phase accumulator generates the phase $\phi\in[0,2\pi)$, with a slope imposed by the frequency control word *FCW*.

In the simplest implementation, the sine and cosine computation blocks are implemented as large look-up tables storing digitized waveforms. Many techniques have been recently developed to improve circuit performance. In [1,2] a piecewise linear approximation is employed, an angle-rotation approach is used in [3], while an advanced ROM compression technique is exploited in [4].

The designed DDFS IC uses the recently proposed Multipartite Table Method [5] (MTM) to calculate trigonometric functions. In MTM the Q-bit input signal x is decomposed in non overlapping sub-words: x_0, x_1, …, x_K of lengths q_0, q_1, ..., q_K respectively. The sub-word x_0, including the most significant bits (MSBs) of x, feeds a table of initial values (TIV) storing a few samples of $f(x)$. Interpolation between TIV samples is performed by summing the outputs of K small tables of offsets (TOs). The i-th TO is addressed by x_i and by a subword ξ_i of x_0, including the p_i MSBs of x_0, with $p_i \le q_0$. Figure 14.3.2 shows the implementation of the MTM for K=2. Exploiting symmetry in the TOs allows the tables to be reduced in size by a factor of two, at the expense of a few XOR gates, as shown in Fig. 14.3.2.

For a given value of K, the optimal values of q_0, …, q_K, p_1, ..., p_K have been obtained in [5] as the ones that minimize the total memory size, while providing an error lower than 1 LSB (*faithful rounding*). However, faithful rounding is not required in DDFS, where the error metric is the SFDR. Therefore we developed a novel algorithm to find the optimal MTM decompositions for the sine and the cosine functions, which minimizes the overall ROM size while providing a target SFDR. To simplify the hardware implementation, the algorithm limits the search space to the decompositions in which the q_i values are the same for sine and cosine functions.

The optimal value of K results from a trade-off between memory size (that reduces with K) and multi operand adder performances. We have found that in our 90dBc design, K=3 is the best choice. The implemented DDFS requires a ROM size of only 1344 bits. As a comparison, a brute force quarter-wave symmetry look-up table requires a ROM size of more than 2.1×10^5 bits. The recent implementation of [4], still employing multi-operand adders, requires a total ROM size of 2176 bits to reach a SFDR of about 80dBc.

Some optimizations are carried out in the implementation of MTM DDFS. From Fig. 14.3.1, x is the output of a 1's complementer. The address bits of the TOs, from Fig. 14.3.2, are in turn obtained by 1's complementing the sub-words of x. As shown in Fig. 14.3.3, these two 1's complementers can actually be replaced by a single modified 1's complementer, which can be shared between the sine and cosine calculation blocks, since the q_i values are the same for the two functions. The conditional 2'complementing of sine and cosine outputs is computed by firstly subtracting 1 LSB (operation embedded in the multi-operand adder) and then performing a 1's complement. The sign-extension prevention technique is extensively used in order to reduce the word-lengths of the multi-operand adder terms. The sign extension prevention constants are precomputed and added to the values stored in the TIV ROM.

The MTM DDFS can easily be pipelined, with maximum clock frequency and total power dissipation strongly affected by flip-flop performances. Unfortunately, there is no flip-flop topology with minimal Power×Delay product for every value of the input switching activity, α. Therefore, we used in our IC two flip-flop topologies. The modified Sense-Amplifier based Flip-flop (SAFF) [6] is very fast, but suffers from high power dissipation for low α values. The Static Ratio Insensitive (SRIS) flip-flop of Yuan and Svensson is a topology that, while being slower than the SAFF, is more efficient for low input switching activities. The power and delay characteristics of the two flip-flop topologies are shown in Fig. 14.3.4. We have not considered flip flops with sizing lower than 0.5×. In fact, an aggressive downscaling of the transistor dimensions to reduce the power dissipation on non-critical paths results in a large dependence of the D-Q delay on the output capacitance, making the timing closure very difficult, since the exact output parasitic values are known only after the detailed routing.

Figure 14.3.5 shows the simulated performance obtained by employing different flip-flop sizes and topologies to implement our DDFS. The required clock frequency of 600MHz is not achieved by using only SRIS flip-flops. By using only SAFFs, the target clock frequency is reached and a reduction of the power dissipation is observed when several flip flop sizes are used. The best solution is obtained by using the two flip-flop topologies together.

The test chip, shown in Fig. 14.3.7, was fabricated in 0.25μm, 2.5V CMOS technology. The die also includes BIST logic to simplify experimental measurements. The DDFS works correctly up to 630MHz at 2.5V, with a power dissipation of 76mW. For a power supply of 1.8V, a maximum frequency of 430MHz was measured, with a power dissipation of 24.9mW.

Figure 14.3.6 compares the performance of the prototype IC with state-of-the-art DDFS implementations. The DDFS uses only a fraction of the area of previous circuits. The power dissipation is also reduced by a factor greater than 3, with respect to previous DDFS with SFDR greater than 80dBc. The DDFS of [4] dissipates 25% more power and is faster than our IC. However, the output resolution and the SFDR of [4] are lower than our design. Moreover two parallel sine generators are used in [4] to increase the maximum clock frequency, with a large area penalty.

Acknowledgements:
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References:
[1] J. M. P. Langlois, D. Al Khalili, "Low Power Direct Digital Frequency Synthesizer in 0.18μm CMOS," *Proc. of Custom IC Conf.*, pp. 21-24, Sept., 2003.
[2] Y. Song, B. Kim, "A 14-b Direct Digital Frequency Synthesizer With Sigma-Delta Noise Shaping," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 847-851, May, 2004.
[3] Y. Song, B. Kim, "Quadrature Direct Digital Frequency Synthesizers Using Interpolation-Based Angle Rotation," *IEEE Trans. on VLSI*, vol. 12, no. 7, pp. 701-710, July, 2004.
[4] B. D. Yang et al. "An 800MHz Low-Power Direct Digital Frequency Synthesizer with on-chip D/A Converter," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 761-774, May, 2004.
[5] F. De Dinechin, A. Tisserand, "Multipartite Table Methods," *IEEE Trans. on Computers*, pp. 319-330, vol. 54, no. 3, Mar., 2005.
[6] A. Strollo et al., "Novel High-Speed Sense-Amplifier based Flip-flops," *IEEE Trans. on VLSI*, accepted for publication.

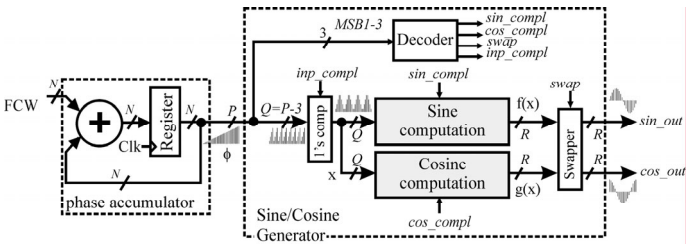

Figure 14.3.1: Simplified schematic of a direct digital frequency synthesizer.

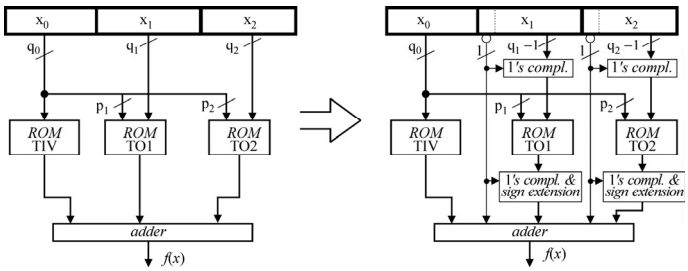

Figure 14.3.2: Multipartite table method using *K*=2 tables of offsets (TOs).

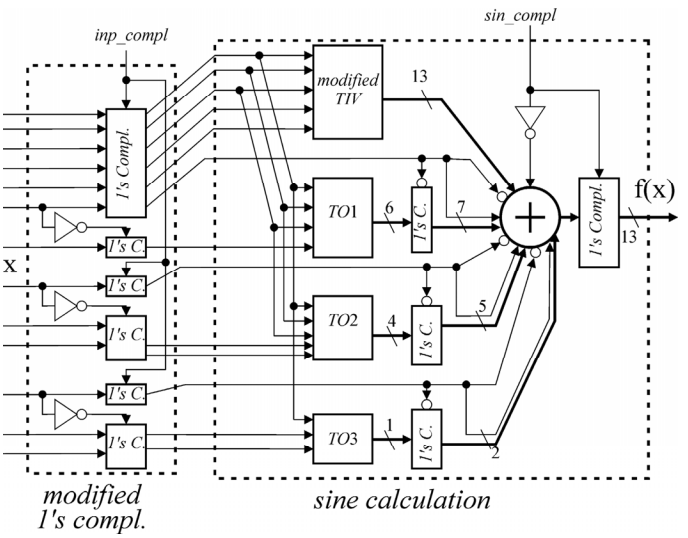

Figure 14.3.3: Detailed implementation of modified 1's complementer and sine computation block.

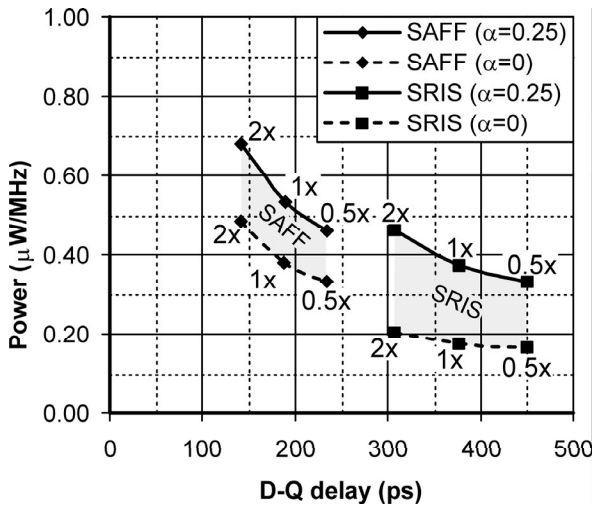

Figure 14.3.4: Characteristics of the employed flip-flops.

Employed Flip-flops	Area (10^3 μm^2)	clock freq. (MHz)	P_D (μW/MHz)
SRIS 2x	79.6	516	147
SAFF 2x	78.9	600	216
SAFF 2x/1x	65.5	600	176
SAFF 2x/1x/05x	59.5	600	157
SAFF 2x/1x/05x + SRIS 2x/1x/05x	63.2	600	130

Figure 14.3.5: Simulated DDFS performances obtained by employing different flip-flop sizes and topologies.

Circuit	Technique	Accum. (bit)	SFDR (dBc)	Pipeline levels	Output	Process (μm)	Area (mm^2)	fclk max (MHz)	Power (μW/MHz)
This paper	Multipartite table with SFDR opt.	32	90	5	13 bits quadrature	0.25	0.063	630	121
Langlois [1] *CICC 2003*	Piecewise linear (32 segments)	32	84	4	12 bits quadrature	0.18	0.090	150	600
Song [2] *JSSC 2004*	Piecewise linear (128 segments)	30 ΣΔ	110	N.A.	14 bits single	0.25	0.120	250	400
Song [3] *TVLSI 2004*	Angle rotation	32	100	9	16 bits quadrature	0.35	1.40	150	2333
Yang [4] *JSSC 2004*	ROM Compression: quad-line approximation two parallel sine generators	32	~ 60	26	9 bits single	0.35	0.440	820	153

Figure 14.3.6: Comparison between DDFS ICs.

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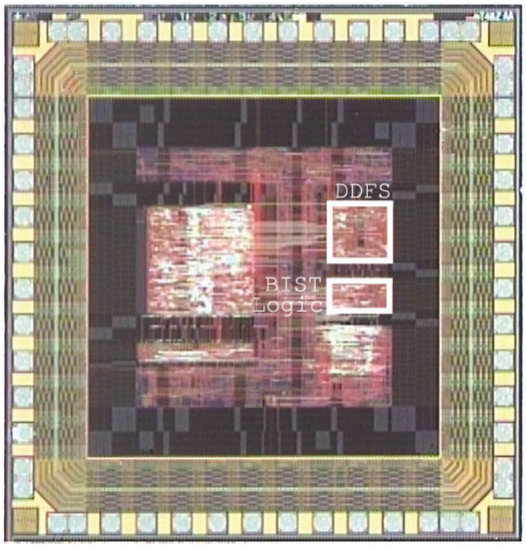

Figure 14.3.7: Test chip micrograph.

